IN THE CLAIMS:

Claim 1 (Currently amended) A method of fabricating a non-volatile memory, comprising the steps of:

providing a substrate;

forming a longitudinal strip of stacked layer over the substrate, wherein the longitudinal strip is a stack that includes a gate dielectric layer, a conductive layer and a cap layer;

forming a buried bit line in the substrate on each side of the longitudinal strip;

patterning the longitudinal strip to form a plurality of stacked blocks;

forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks;

removing the cap layers of some of the stacked blocks ~~so that~~ to form a plurality of first opening exposing a portion of the conductive layer of the stacked blocks ~~is exposed~~; and

forming a word line over the dielectric layer and filling the first openings to connect the portion of the conductive layer exposed by the first opening of the stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having the word line connecting to the conductive layer of the stacked blocks are in a first data state and the coding memory cells having the word line connecting to the cap layers of the stacked blocks are in a second data state.

Claim 2 (Currently amended) The method of claim 1, wherein the cap layer has an etching rate greater than the dielectric layer when removing the cap layers of some of the stacked blocks.

Claim 3 (Original) The method of claim 1, wherein material constituting the cap layer includes silicon oxide.

Claim 4 (Original) The method of claim 1, wherein material constituting the dielectric layer includes silicon nitride.

Claim 5 (Original) The method of claim 1, wherein material constituting the word line includes metallic substance or polysilicon.

Claim 6 (Original) The method of claim 1, wherein material constituting the conductive material includes polysilicon.

Claim 7 (Original) The method of claim 1, wherein the step of forming the buried bit line includes conducting an ion implantation using the longitudinal strip as an implant mask.

Claim 8 (Currently amended) The method of claim 1, wherein the step of removing the cap layers of some stacked blocks includes the sub-steps of:

forming a code-masking layer over the dielectric layer, wherein the code-masking layer has a plurality of second openings substantially aligned to and exposing ~~expose~~ the cap layers of some stacked blocks;

conducting an anisotropic etching process to remove the cap layers exposed by the second openings so as to form the first openings; and

removing the code-masking layer.

Claim 9 (Currently amended) The method of claim 8, wherein the anisotropic etching process includes a wet etching process or a dry etching process.

Claim 10 (Previously Withdrawn) A non-volatile memory structure, comprising:

a substrate;

a buried bit line within the substrate;

a plurality of first stacked blocks on the substrate, wherein each first stacked block is a stack having a cap layer, a conductive layer and a gate dielectric layer;

a plurality of second stacked blocks on the substrate, wherein each second stacked block is a stack having a conductive layer and a gate dielectric layer;

a dielectric layer over the substrate for isolating the first stacked blocks and the second stacked blocks; and

a word line over the dielectric layer for connecting stacked blocks in the same row serially to form a plurality of coding memory cells, wherein the coding memory cells having a first stacked block is in a first data state and the coding memory cells having a second stacked block is in a second data state.

Claim 11 (Previously Withdrawn) The structure of claim 10, wherein material constituting the cap layer includes silicon oxide.

Claim 12 (Previously Withdrawn) The structure of claim 10, wherein material constituting the dielectric layer includes silicon nitride.

Claim 13 (Previously Withdrawn) The structure of claim 10, wherein material constituting the word line includes metallic substance or polysilicon.

Claim 14 (Previously Withdrawn) The structure of claim 10, wherein material constituting the conductive material includes polysilicon.

Claim 15 (Currently added) The method of claim 1, wherein the step of forming the dielectric layer includes the sub-steps of:

depositing a dielectric material layer over the substrate; and

removing a portion of the dielectric layer until the cap layer are exposed.

Claim 16 (Currently added) The method of claim 15, wherein the step of removing a portion of the dielectric layer includes an etching back process or a chemical-mechanical polishing process.

Claim 17 (Currently added) A method of fabricating a mask read-only-memory, the mask read-only-memory including a plurality of coding memory cells having a first data state and a second data state respectively, comprising the steps of:

providing a substrate;

forming a plurality of buried bit lines in the substrate;

forming a plurality of stacked blocks between each adjacent two buried bit lines, wherein each stacked block includes a gate dielectric layer and a conductive layer;

performing a coding process by means of forming a plurality of insulator layers on a portion of the stacked blocks and forming a plurality of conductive pillars on the stacked blocks without forming the insulator layer thereon; and

forming a plurality of word lines, wherein each word line contacts the conductive layer and the insulator layers in the same row serially to form the coding memory cells, and the coding memory cells having the word line contacting to the conductive pillars are in the first data state and the coding memory having the word line contacting to the insulator layer are in the second data state.

Claim 18 (Currently added) The method of claim 17, wherein the step of performing the coding process includes the steps of:

forming a plurality of cap layer on the conductive layer of each stacked gate;

forming a dielectric layer over the substrate, wherein the dielectric layer exposes the cap layers of the stacked blocks;

forming a code-masking layer over the dielectric layer, wherein the code-masking layer has a plurality of first openings substantially aligned to and exposing the cap layers;

removing the cap layers exposed by the first openings to form a plurality of second openings exposing a portion of the conductive layer of the stacked blocks;

removing the code-masking layer; and

forming a plurality of conductive plugs in the second openings to form the conductive pillars.

Claim 19 (Currently added) The method of claim 18, wherein the step of forming the dielectric layer includes the sub-steps of:

depositing a dielectric material layer over the substrate; and

removing a portion of the dielectric layer until the cap layer are exposed.

Claim 20 (Currently added) The method of claim 19, wherein the step of removing a portion of the dielectric layer includes an etching back process or a chemical-mechanical polishing process.

Claim 21 (Currently added) The method of claim 18, wherein the cap layer has an etching rate greater than the dielectric layer when removing the cap layers exposed by the first openings.

Claim 22 (Currently added) The method of claim 21, wherein material constituting the cap layer includes silicon oxide and the dielectric layer includes silicon nitride.

Claim 23 (Currently added) The method of claim 18, wherein the step of removing the cap layer is performed by an anisotropic etching process.

Claim 24 (Currently added) The method of claim 23, wherein the anisotropic etching process includes a wet etching process or a dry etching process.

CONCLUSION

It is believed that all pending claims 1-9 and 15-24 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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